prior art

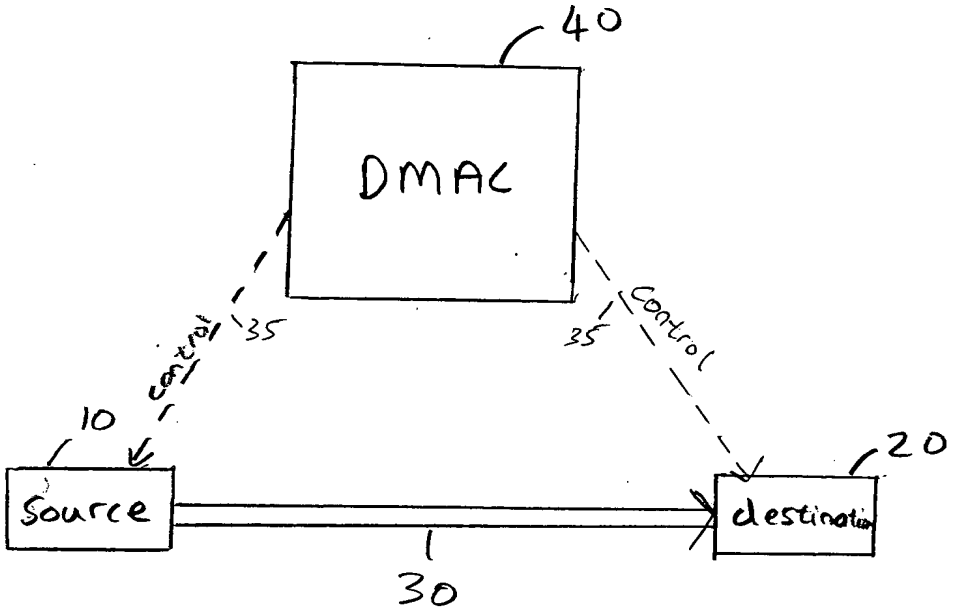


Fig 1

prior art

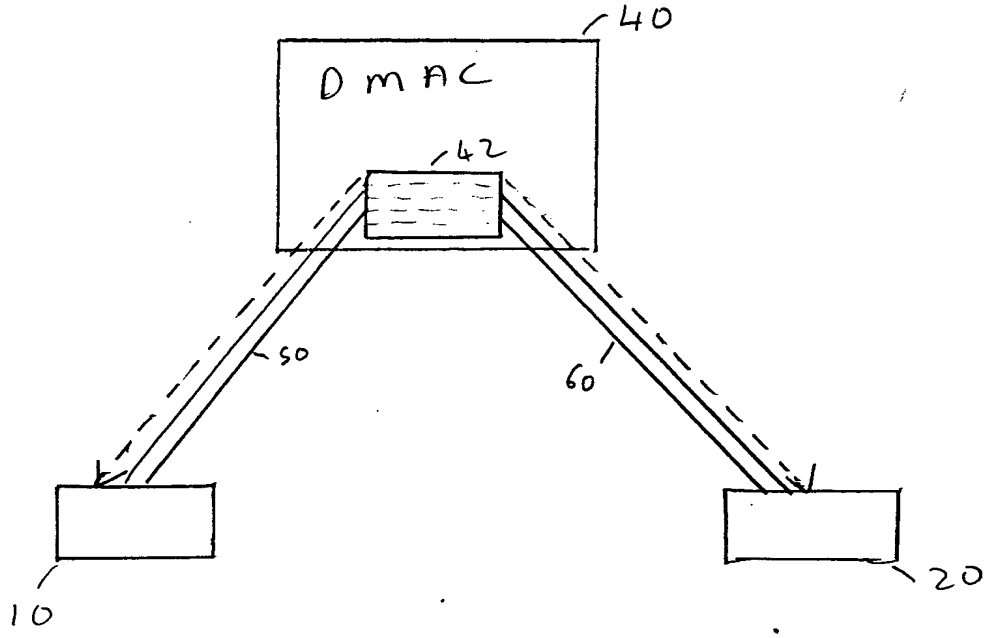


Fig 2

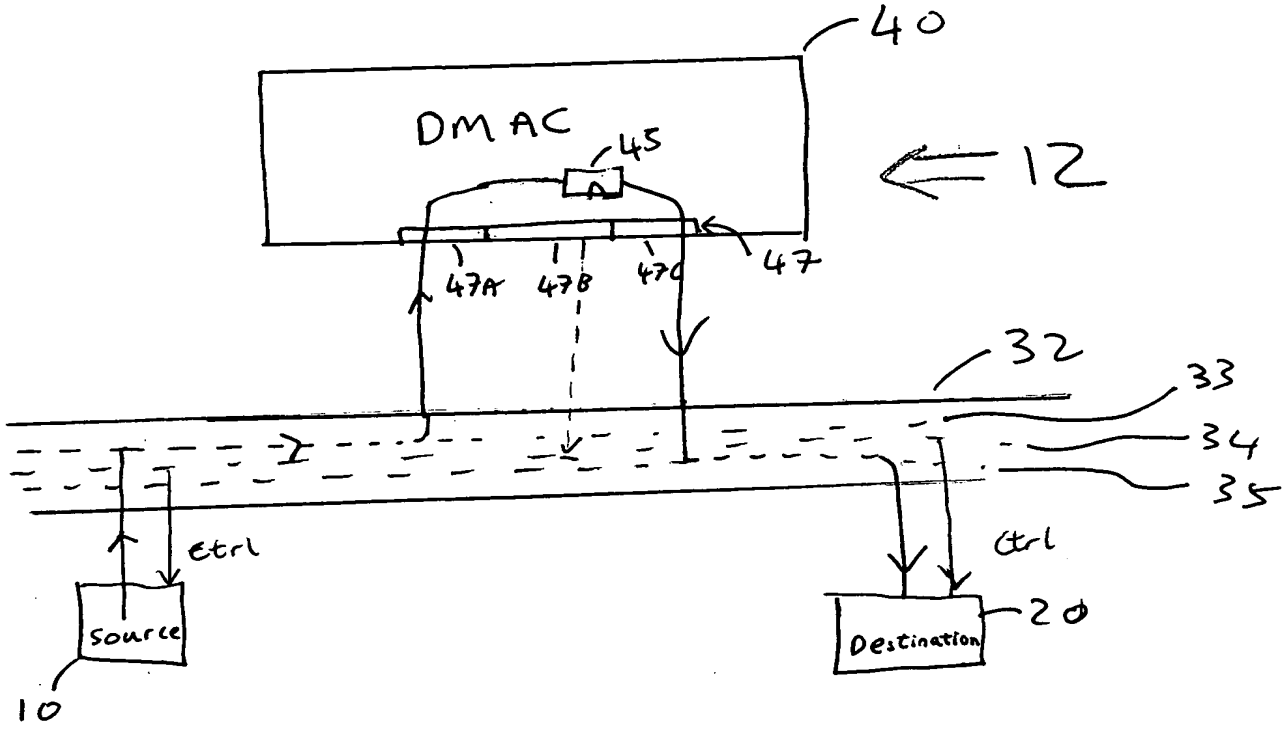
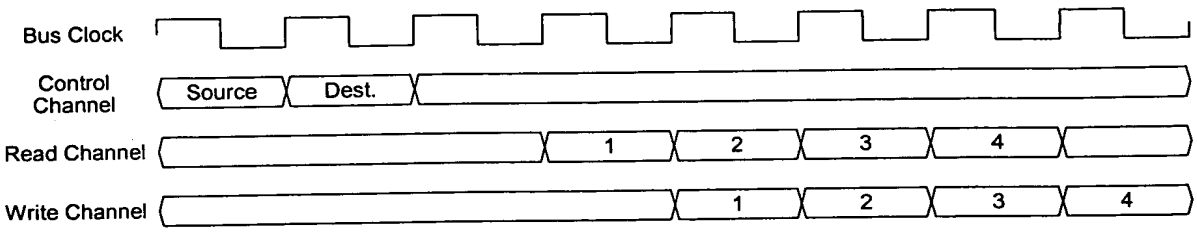

40
DMAC
45
12
47A
47B
47C
47
32
33
34
35
Ctrl
Ctrl
Source
Destination
20
10

Fig 3



Example showing 1-cycle delay through DMAC

The DMAC issues the control sequence for the source burst ("Source"), then at some later point issues the control sequence for the destination burst ("Dest.") - these are shown in adjacent cycles in this example.

The source services the source burst by placing data items on the read channel. These are delayed by one cycle before being placed onto the write channel by the DMAC.

Figure 4

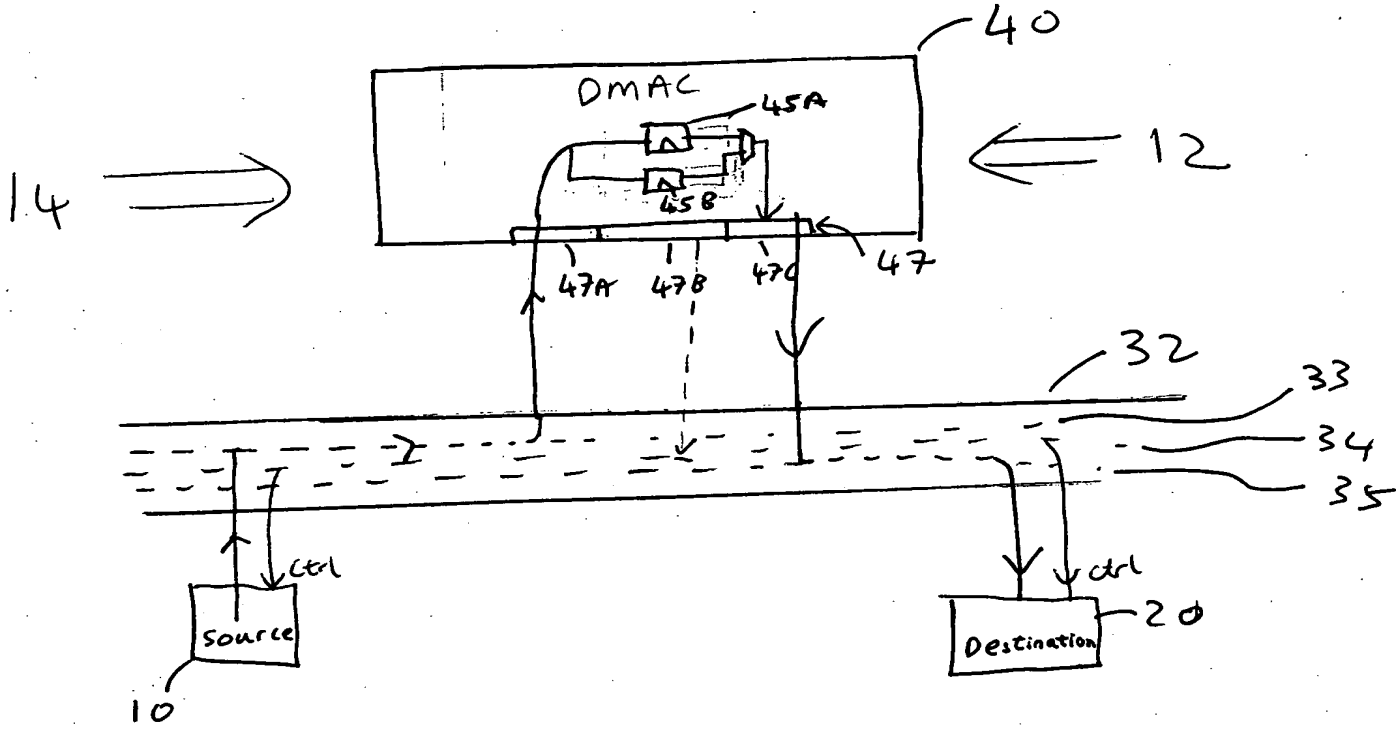

40
DMAC
45A
45B
12
14
47A
47B
47C
47
32
33
34
35
ctrl
ctrl
source
Destination
20
10

Figure 5

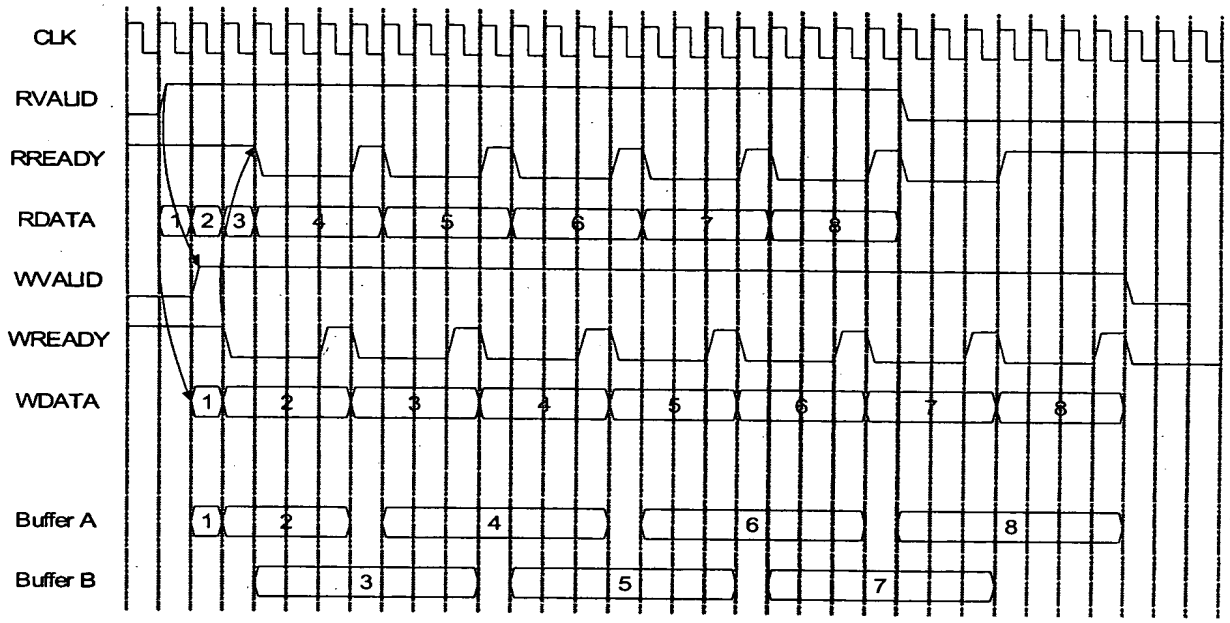

CLK
RVALID
RREADY
RDATA
WVALID
WREADY
WDATA
Buffer A
Buffer B
1
2
3
4
5
6
7
8

Figure 6

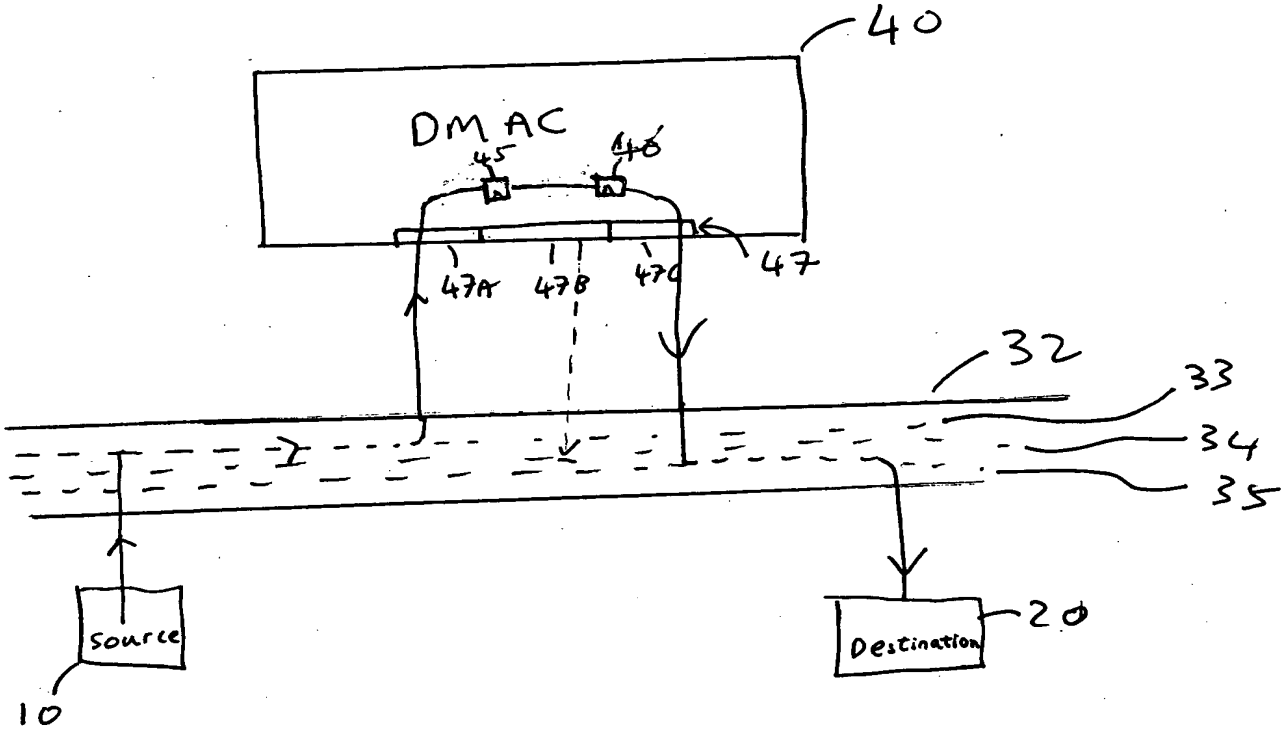

40
DMAC
45
46
47
47A
47B
47C
32
33
34
35
Source
10
Destination
20

Fig 7

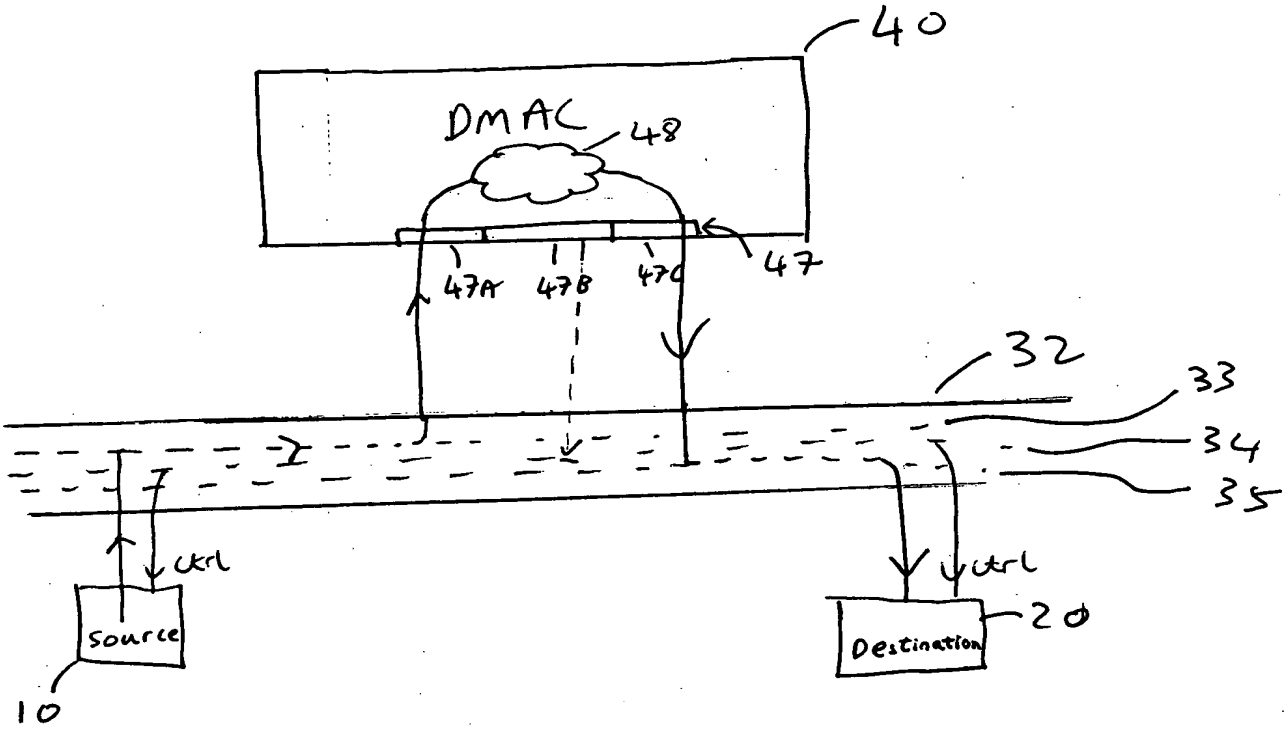

40
DMAC
48
47
47A
47B
47C
32
33
34
35
Ctrl
Ctrl
Source
Destination
20
10

Figure 8

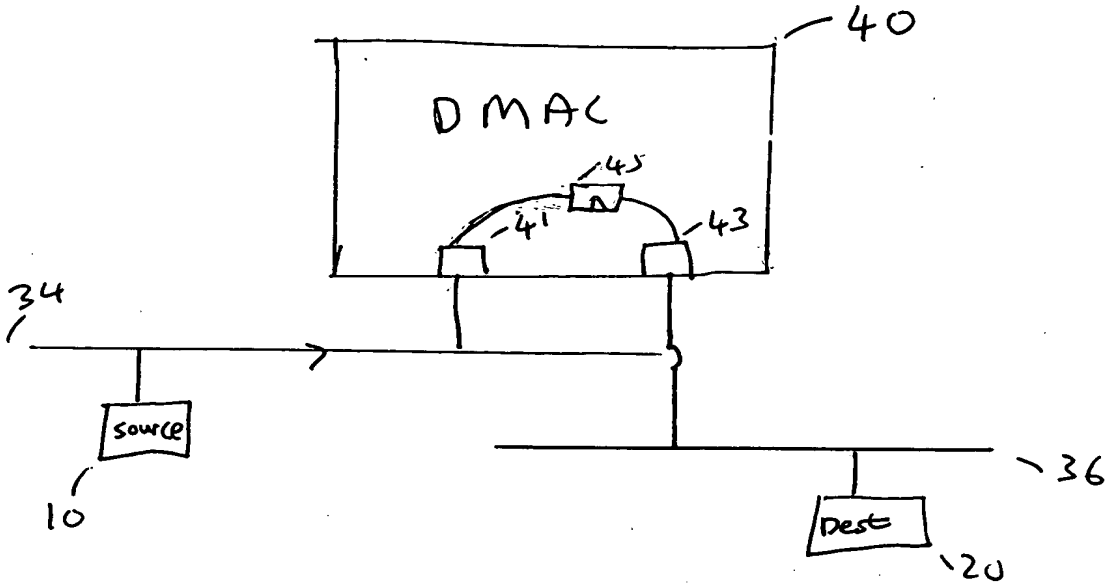


Fig 9